Toyoda Gosei Co., Ltd.

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Vertical GaN Power Device With Current Operation of 100 Amperes

Background

The environmental and energy problems of recent years have led to growing needs for energy savings and electrification. Power semiconductors, especially those with large power capacity, have been a focus of considerable attention among the electronics components that are essential for power conversion. Interest is also being directed toward gallium nitride (GaN), which has material properties superior to silicon for these power semiconductors.

Research and investigations of practical application of power semiconductors using GaN have advanced rapidly in recent years. With AlGaN/GaN based lateralfield effect transistors (FETs) , low on-resistance has been achieved with high-mobilitytwo-dimensional electron gas. These lateral FETs can be made at low cost with the use of an Si substrates, which are inexpensive and can have large diameters. However, maintaining a high withstanding voltage with the lateral FET requires a substantial spacingbetween the gate and drain. This makes the chip size larger, which leads to difficulties in reducing size and increasing integration.

Toyoda Gosei has been developing a vertical GaN power semiconductor device using a GaN substrate. Smaller size and higher integration are relatively easy with vertical FETs, since the withstanding voltage is maintained by the thickness of the drift layer. After designing cells with a honeycomb structure in semiconductor chips, our development efforts have been focused on low resistance, high withstanding voltage vertical GaN-MOSFET using wiring technology for parallel operation and cell miniaturization and higher integration.

Recently, for even lower resistance, we have adopted a structure that inserts a current distribution layer (CDL) between the semiconductor layers. This has allowed us to achieve a high current operation of 100 amperes on a single chip by expanding the current in the drift layer and lowering the resistance.

Explanation of recent development

1. Use of a current distribution layer

Electrons in FETs flow from the source region to drain via a channel and drift layer. When electrons flow from the channel (pGaN) to drift layer, there is a certain amount of expansion as they move toward the drain. Thus, electrons flow in a narrow region near the channel and over a wider region near the drain. This means that in the immediate vicinity of the channel, electron pathways exist in a narrow region of the drift layer, with correspondingly high resistance. By inserting a CDL, these electron pathways can widen this narrow region. As a result, lower resistance can be obtained (Fig. 1).

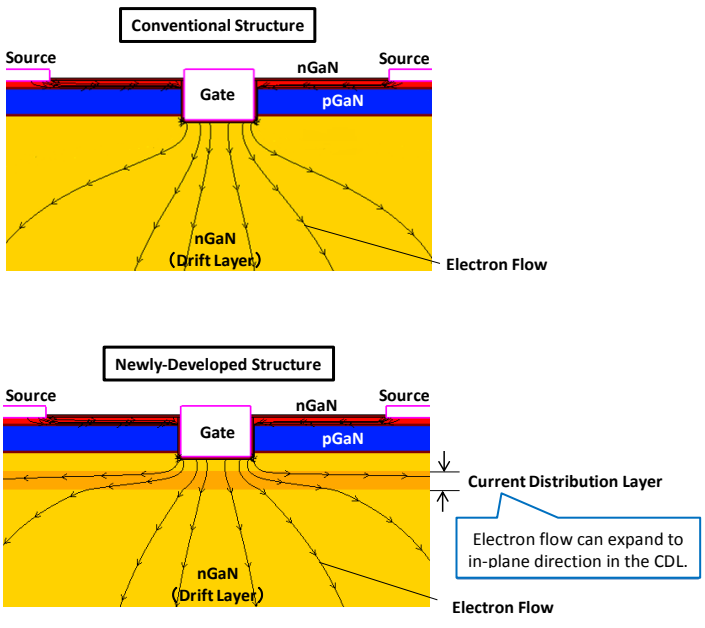

Fig. 1. Diagram of the cross-sectional structure of vertical GaN-MOSFET.

2. Optimizing structure through simulations

Investigations were also made into where the CDL should be positioned. For lower resistance, it is better to expand the electron pathways in the drift layer at an early stage; that is, at a location as close to the channel as possible. However, since a region with few majority carriers (depletion layer) is formed near the pn junction interface, a high impurity concentration needs to be formed when forming the CDL forms in the pn junction interface a layer. In such cases, the electric field strength of the pn junction interface in an off-state condition becomes higher, leading to the contrary result of poorer withstanding voltage. Toyoda Gosei therefore investigated where the CDL should be formed, and from simulations discovered a position where the current distribution effect is high and less susceptible to the effects of the depletion layer, and a high withstanding voltage can be maintained (Fig. 2).

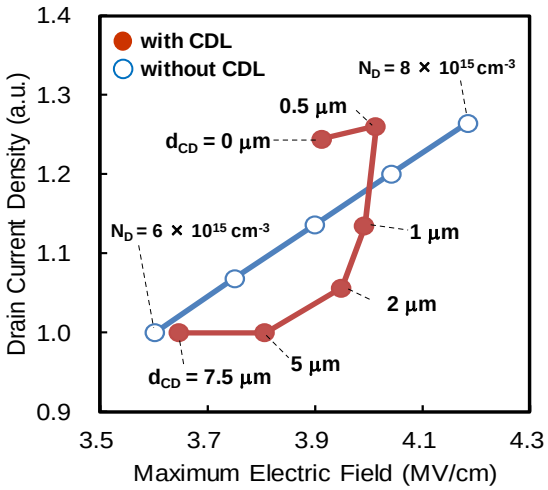

Fig. 2. Relationship between positioning of current distribution layer, drain current density, and maximum electric field strength in the region of concentrated electric field.

3. World class large current operation on a single chip

We fabricated and tested small-element vertical GaN-MOFSETs with and without the CDL from the results of the above simulations, and in a comparison using a drain voltage of 0.5 V and gate voltage of V_{th} + 20 V, we confirmed that by inserting a CDL the drain current becomes 1.17 times higher (Fig. 3), whereas the withstanding voltages were confirmed to be the same. As a demonstration of large current operation, chips using a CDL were fabricated and confirmed to have large current operation of 100 A on a single chip (Fig. 4).

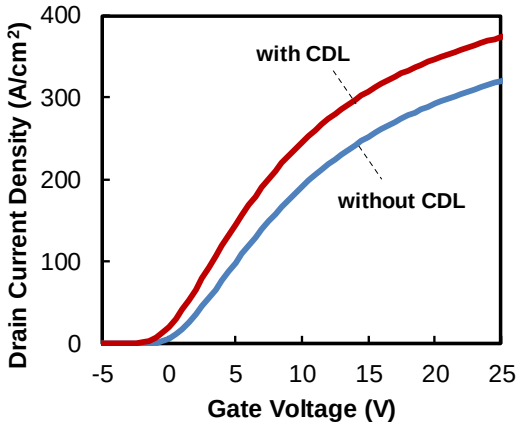

Fig. 3. Id-Vgs characteristics of vertical MOFSET.

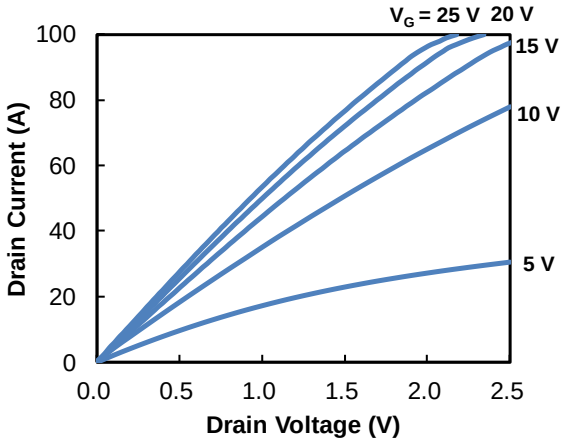

Fig. 4. Id-Vds characteristics of vertical MOFSET with a current distribution layer.

Future outlook

Toyoda Gosei will continue striving for further improvements, including greater reliability, for early actualization of high performance power semiconductors.